AMENDMENT TO RULES COMM. PRINT 119–33
OFFERED BY MR. HUIZENGA OF MICHIGAN

Add at the end of subtitle A of title XVII the following:

SEC. 17___. CHIP SECURITY.

(a) INITIAL REPORT TO CONGRESS ON CHIP SECURITY MECHANISMS.—

(1) ASSESSMENT.—On the date of the enactment of this Act, the Secretary, in consultation with the Secretary of State, the Secretary of Defense, and the Secretary of Energy and in robust consultation with the public in a manner determined appropriate by the Secretary and in consultation with the heads of other relevant Federal departments and agencies, shall initiate an assessment to—

(A) identify potential chip security mechanisms to enable reliable verification of whether a covered integrated circuit product has been illegally diverted or accessed;

(B) develop incentives for facilitating industry-wide incorporation of such chip security mechanisms;

(C) conduct an analysis of the potential costs associated with implementing such chip security mechanisms; and

(D) recommend a set of chip security mechanisms that would effectively detect diversion and smuggling and is technically feasible, cost-effective, and ensures the technology leadership of the United States.

(2) STAKEHOLDER ENGAGEMENT.—In carrying out the requirements under paragraph (1), the Secretary shall undertake a robust stakeholder engagement process to inform the development and implementation of chip security mechanisms, which shall include—

(A) soliciting input from relevant stakeholders, including—

(i) private sector entities involved in the covered integrated circuit product supply chain;

(ii) experts in software, firmware, hardware security, cybersecurity, privacy, export compliance, national security, and advanced artificial intelligence; and

(iii) individuals from academic institutions, federally funded research and devel-

opment centers, Federal departments and agencies, and other research organizations with relevant expertise; and

(B) incorporating stakeholder feedback to ensure that required chip security mechanisms are operationally effective, scalable, and aligned with best practices in security, privacy, and export compliance.

(3) REPORT TO CONGRESS.—

(A) IN GENERAL.—Not later than 210 days after the date of the enactment of this Act, the Secretary shall submit to the appropriate congressional committees a report on the results of the assessment required by paragraph (1), including—

(i) an identification of the chip security mechanisms the Secretary plans to propose pursuant to implementing subsection (b);

(ii) an identification of future research and development directions that could be used to enhance robustness of chip security mechanisms and incentives to promote such research and development directions;

(iii) a roadmap for the timely implementation of the chip security mechanisms; and

(iv) any recommendations for potential modifications to relevant export controls to allow for more flexibility with respect to the countries to or in which covered integrated circuit products may be exported, reexported, or in-country-transferred if the products include chip security mechanisms.

(B) FORM.—The report required in this paragraph shall be submitted in unclassified form but may include a classified annex.

(b) REQUIREMENTS FOR CHIP SECURITY MECHANISMS FOR EXPORT, RE-EXPORT, OR IN-COUNTRY TRANSFER OF COVERED INTEGRATED CIRCUIT PRODUCTS.—

(1) PRIMARY REQUIREMENTS.—

(A) IN GENERAL.—Not later than one year after the date of the enactment of this Act, the Secretary, in consultation with the Secretary of State, the Secretary of Defense, and the Secretary of Energy, shall require any covered integrated circuit product that is exported, reexported, or in-country-transferred to or within a

foreign country to be secured by a chip security mechanism that enables reliable verification of whether the product has been illegally diverted to destinations of concern, to the extent consistent with the recommendations submitted pursuant to section (a)(3), using techniques that are feasible and appropriate on such date of enactment.

(B) VARYING MECHANISMS PERMITTED.—In implementing the requirements of subparagraph (A), the Secretary may require chip security mechanisms that vary by geographical region and by party, as the Secretary deems appropriate in light of national security interests, foreign policy objectives, and the assessment of the Secretary of the risk of diversion.

(C) PROPOSED REGULATIONS.—

(i) IN GENERAL.—Not later than 270 days after the date of the enactment of this Act, the Secretary shall promulgate proposed regulations implementing the requirements of subparagraph (A).

(ii) REQUIREMENTS.—In promulgating the proposed regulations under clause (i), the Secretary shall—

(I) solicit public feedback on potential guidance to clarify the categories of persons subject to this requirement, how information should be securely shared between entities, and the procedures for submission of such notifications, in order to ensure clarity regarding compliance obligations and implementation; and

(II) propose and clarify how the regulations can be applied in nations with data localization laws or data privacy laws, providing flexibility if such laws require novel or flexible approaches.

(D) FINAL RULE.—Not later than one year after the date of the enactment of this Act, the Secretary, in robust consultation with the public in a manner determined appropriate by the Secretary and in consultation with the heads of other relevant Federal departments and agencies, shall promulgate a final rule that may include a reporting requirement to inform the Bureau of Industry and Security of the Department of Commerce whenever chip security

mechanisms fail to confirm that any covered integrated circuit product has not been illegally diverted to a destination of concern, taking into account reasonable time for persons to verify or repair the chip security mechanism, identified in the final rule, including instances in which there is evidence that a product has been subjected to tampering or an attempt at tampering, including efforts to disable, spoof, falsify, manipulate, mislead, or circumvent chip security mechanisms.

(E) STAKEHOLDER ENGAGEMENT.—In carrying out this paragraph, the Secretary should undertake a robust stakeholder engagement process to inform the development and implementation of chip security mechanisms, which shall include—

(i) soliciting input from relevant stakeholders, including—

(I) private sector entities involved in the covered integrated circuit product supply chain;

(II) experts in software, firmware, and hardware security, cybersecurity, privacy, export compli-

ance, national security, and advanced artificial intelligence; and

(III) individuals from academic institutions, federally funded research and development centers, Federal departments and agencies, and other research organizations with relevant expertise; and

(ii) incorporating stakeholder feedback to ensure that required chip security mechanisms are operationally effective, scalable, and aligned with best practices in security, privacy, and export compliance.

(2) ENHANCEMENTS TO CHIP SECURITY MECHANISMS.—

(A) ASSESSMENT.—

(i) IN GENERAL.—Not later than two years after the date of the enactment of this Act, and annually thereafter for three years, the Secretary, in consultation with the Secretary of State, the Secretary of Defense, and the Secretary of Energy, shall—

(I) conduct an assessment, in robust consultation with the public in a

manner determined appropriate by the Secretary and in consultation with the heads of other relevant Federal departments and agencies, to identify what enhancements, if any, should be used to improve the chip security mechanisms implemented under paragraph (1)(A)—

(aa) to enhance compliance with the requirements of the Export Control Reform Act of 2018 (50 U.S.C. 4801 et seq.);

(bb) to detect the illegal diversion of covered integrated circuit products;

(cc) to identify and monitor smuggling intermediaries;

(dd) to ensure United States technology leadership;

(ee) to ensure the orderly and effective implementation of the chip security mechanism; and

(ff) to address industry feedback about the implementation of the chip security mechanism;

(II) if the Secretary identifies any such enhancements, develop incentives for facilitating industry-wide incorporation of such enhancements for covered integrated circuit products; and

(III) where necessary, to expedite the implementation of such enhancements and identify and support research activities, such as—

(aa) updating and clarifying relevant vulnerability and threat models;

(bb) developing definitions, assets, and other practices to support traceability and provenance of materials and data across the product lifecycle;

(cc) developing updated databases of existing trust and assurance data practices; and

(dd) developing practices for implementing chip security mechanisms and sharing relevant information across the product life

cycle while protecting confidential intellectual property.

(ii) ELEMENTS.—The assessment required by clause (i) shall include—

(I) an examination of the feasibility, reliability, and effectiveness of—

(aa) methods and strategies that prevent the tampering, disabling, or other manipulating of covered integrated circuit products; and

(bb) any other method the Secretary determines appropriate for the prevention of unauthorized use, access, or exploitation of covered integrated circuit products;

(II) an analysis of—

(aa) the potential costs associated with implementing each method examined under subclause (I), including an analysis of—

(AA) the potential impact of the method on the performance of covered integrated circuit products; and

(BB) the potential for the introduction of new vulnerabilities into the products;

(bb) the potential benefits of implementing the methods examined under subclause (I), including an analysis of the potential increase—

(AA) in compliance of covered integrated circuit products with the requirements of the Export Control Reform Act of 2018 (50 U.S.C. 4801 et seq.);

(BB) in detecting and deterring illegal diversion of the covered integrated circuit products; and

(CC) in enhancing persons' global inventory management; and

(cc) the susceptibility of the methods examined under subclause (I) to tampering, disabling, or other forms of manipulation; and

(III) an estimate of the expected costs to implement at-scale methods to tamper with, disable, or manipulate a covered integrated circuit product, or otherwise circumvent the methods examined under subclause (I).

(B) REPORT TO CONGRESS.—

(i) IN GENERAL.—Not later than two years after the date of the enactment of this Act, and annually thereafter for three years, the Secretary shall submit to the appropriate congressional committees a report on the results of the assessment required by subparagraph (A), including—

(I) an identification of the chip security mechanisms, if any, to be in-

cluded in the requirements for enhanced chip security mechanisms;

(II) an identification of research and development directions that could be used to improve the robustness of chip security mechanisms and incentives to promote such research and development directions;

(III) if applicable, a roadmap for the timely implementation of the enhanced chip security mechanisms; and

(IV) any recommendations for modifications to relevant export controls to allow for more flexibility with respect to the countries to or in which covered integrated circuit products may be exported, reexported, or in-country-transferred if the products include enhanced chip security mechanisms.

(ii) FORM.—The report required by subparagraph (A) shall be submitted in unclassified form, but may include a classified annex.

(C) IMPLEMENTATION.—

(i) IN GENERAL.—If any enhanced chip security mechanisms identified pursuant to subparagraph (A)(i) are determined by the Secretary to be appropriate, the Secretary may, not later than two years after the date on which the Secretary completes the assessment required by subparagraph (A), require any covered integrated circuit product to incorporate the enhanced chip security mechanisms, or for additional mechanisms to be otherwise implemented, at the time the product is exported, reexported, or in-country transferred to or in a foreign country.

(ii) PRIVACY AND CYBERSECURITY.—In assessing and developing requirements for enhanced chip security mechanisms under this paragraph, the Secretary shall prioritize mitigation of confidentiality and cybersecurity risk.

(3) ENFORCEMENT AUTHORITY.—In addition to the penalty and enforcement authorities granted to the Secretary under the Export Control Reform Act of 2018 (50 U.S.C. 4801 et seq.) or otherwise pro-

vided by law, in carrying out this subsection, the Secretary may—

(A) verify, in a manner the Secretary determines appropriate, the ownership and location of a covered integrated circuit product that has been exported, reexported, or in-country transferred to or in a foreign country;

(B) maintain a record of covered integrated circuit products and include in the record the location and current end-user of each such product; and

(C) require any person involved in the design, manufacture, sale, physical security, oversight, distribution, export, or licensed transfer of a covered integrated circuit product being exported, re-exported, or in-country-transferred to a foreign country to provide the information needed to maintain the record (such as essential information relating to the chip security mechanisms, or the end-user of covered integrated circuit products located outside of the United States).

(4) FOREIGN COMPETITIVENESS ASSESSMENT AND RELATED AUTHORITIES.—

(A) IN GENERAL.—The Secretary shall annually assess the competitiveness of foreign covered integrated circuit products in relation to United States covered integrated circuit products.

(B) WAIVER.—The Secretary, in consultation with the Secretary of State, the Secretary of Defense, and the Secretary of Energy, is authorized to waive any requirements of this section if the Secretary, in consultation with such Secretaries, determines that the implementation of chip security mechanisms poses an undue burden on United States competitiveness, is inconsistent with the national security interests of the United States, and that exercising any and all authorities under the Export Control Reform Act of 2018 (50 U.S.C. 4801 et seq.) insufficiently addressed issues arising from the presence of sufficient volume of foreign covered integrated circuit products not covered by the requirements of this section.

(C) CONGRESSIONAL NOTIFICATION.—At least 30 days prior to exercising the waiver described in subparagraph (B), the Secretary shall provide a written notification to the appro-

priate congressional committees containing detailed quantitative analysis demonstrating the rationale for the waiver and that exercising any and all authorities under the Export Control Reform Act of 2018 (50 U.S.C. 4801 et seq.) insufficiently addressed issues arising from the presence of sufficient volume of foreign covered integrated circuit products not covered by the requirements of this section.

(5) ENFORCEMENT.—A violation of any provision of this section, or of any regulation, order, license, or other authorization issued pursuant to this section shall be deemed a violation of the Export Control Reform Act of 2018 (50 U.S.C. 4801 et seq.).

(6) ADMINISTRATIVE PROCEDURES.—The provisions of section 1761(h) and section 1762 of the Export Control Reform Act of 2018 (50 U.S.C. 4801 et seq.) shall apply to this section in the same manner and to the same extent as such provisions apply to the Export Control Reform Act of 2018.

(c) RULES OF CONSTRUCTION.—Nothing in this section may be construed to direct the Secretary to—

(1) require any chip security mechanisms that may hinder the capability or functionality of a cov-

ered integrated circuit product, such as a kill switch or geofencing mechanism, or meaningfully undermine the cybersecurity of the covered integrated circuit product;

(2) mandate the incorporation of a location verification mechanism on a covered integrated circuit product that requires physical changes to hardware;

(3) consider any chip security mechanism requirements of this section as applicable to a person that fabricates covered integrated circuit products, unless the person also designs the respective covered integrated circuit products;

(4) require chip security mechanisms for exports of integrated circuits, computers, electronic assemblies, or components that are not designed or marketed for artificial intelligence datacenter use;

(5) limit any other enforcement authority of the Secretary or the head of any other Federal department or agency under the Export Control Reform Act of 2018 (50 U.S.C. 4801 et seq.) or any other provision of law; or

(6) apply any requirements or regulations under this section to any covered integrated circuit products in the United States.

(d) ASSESSMENT OF THE PEOPLE'S REPUBLIC OF CHINA'S MILITARY USE OF ARTIFICIAL INTELLIGENCE.—

(1) IN GENERAL.—Not later than 180 days after the date of the enactment of this Act, and annually thereafter, the Secretary of Defense shall submit to the Committee on Armed Services and the Committee on Foreign Affairs of the House of Representatives and the Committee on Armed Services and the Committee on Foreign Relations of the Senate a report on the People's Liberation Army Rocket Force use of artificial intelligence, including—

(2) REPORT CONTENTS.—The report required in paragraph (1) shall include a detailed explanation of how the People's Liberation Army Rocket Force is using artificial intelligence for its modernization efforts and force posture in the Western Pacific, including how the People's Liberation Army Rocket Force is exploiting access to United States and allied advanced semiconductor technologies and artificial intelligence.

(3) FORM.—The report required in paragraph (1) shall be submitted in unclassified but may include a classified annex.

(e) DEFINITIONS.—In this section:

(1) The term ''appropriate congressional committees'' means—

(A) the Committee on Banking, Housing, and Urban Affairs of the Senate;

(B) the Committee on Energy and Commerce of the House of Representatives; and

(C) the Committee on Foreign Affairs of the House of Representatives.

(2) The term ''chip security mechanism'' means a software-, firmware-, or hardware-enabled security mechanism or a physical security mechanism, including—

(A) periodic on-site audits or inventories at the end-user's approved destination for the covered integrated circuit product;

(B) periodic attestations by a United States-headquartered entity, a subsidiary of a United States-headquartered entity, or an entity determined by the Secretary to be reliable, confirming that all covered integrated circuit products are accounted for, provided the Secretary determines that the United States-headquartered entity or its subsidiaries verifiably certifies that the United States-headquartered entity or its subsidiaries main-

tain continuous and sufficiently secure control, operation, repair (to the extent such repair is conducted by or under the direct supervision of the United States-headquartered entity or its subsidiaries), and disposal of the covered integrated circuit products;

(C) ping-based location verification through a trusted landmark server utilizing secure software- or firmware-enabled mechanisms; or

(D) various other mechanisms, or combinations of mechanisms, that the Secretary determines can verifiably demonstrate with significant confidence that the covered integrated circuit product has not been illegally diverted to a destination of concern.

(3)(A) The term ''covered integrated circuit product'' means a certain integrated circuit, computer, or other product classified under Export Control Classification Number 3A090, 4A090, 5A002.z, related .z Export Control Classification Numbers, or other functionally equivalent or substantially similar items.

(B) The Secretary shall routinely modify the definition of the term ''covered integrated circuit

product'' under subparagraph (A) for the purposes of this section to ensure only integrated circuits, computers, electronic assembly, or components designed or marketed for datacenter use are subject to the requirements of this section.

(C) The term ''covered integrated circuit'' does not include—

(i) covered integrated circuits or products containing a covered integrated circuit that are not designed or marketed for use in a data center;

(ii) microprocessor microcircuits, such as central processing units, that are not graphics processing units or similar products; or

(iii) network switch integrated circuits whose dominant function is routing traffic over a computing network.

(4) The term ''destination of concern'' means—

(A) a country subject to a United States arms embargo pursuant to section 126.1 of title 22, Code of Federal Regulations; or

(B) any other country determined by the Secretary.

(5) The terms ''export'', ''in-country transfer'', and ''reexport'' have the meanings given those terms

in section 1742 of the Export Control Reform Act of 2018 (50 U.S.C. 4801).

(6) The term ''Secretary'' means the Secretary of Commerce.